CLAIMS:

1. A transimpedance amplifier, comprising:

a differential amplifier having an input and a first and second output;

a low pass filter operatively responsive to said amplifier outputs; and

an automatic gain control circuit to couple across the input and outputs of said differential amplifier to control impedance of said differential amplifier, said automatic gain control circuit comprising a direct current gain amplifier and a first peak detector to couple between said amplifier outputs and said direct current gain amplifier, and a second peak detector to couple between said direct current gain amplifier and said low pass filter.

2. The transimpedance amplifier of claim 1, wherein said amplifier input is a first amplifier input, said amplifier further comprising a second amplifier input and an offset control circuit operatively responsive between said amplifier outputs and said second amplifier input for correcting offset associated with said differential amplifier, said offset control circuit including an integrator operatively responsive to said low pass filter for integrating a first and second outputs from said low pass filter.

3. The transimpedance amplifier of claim 2, wherein said offset control circuit further comprising a transistor connected to said integrator and said second amplifier input, said transistor configured to have a current proportional to an offset associated with said differential amplifier.

4. The transimpedance amplifier of claim 1, wherein said automatic gain control circuit further comprises a gain control transistor to couple between said differential amplifier and said direct current gain amplifier.

5. The transimpedance amplifier of claim 4, wherein said gain control transistor includes a first gain control transistor, said automatic gain control circuit further comprising a second gain control transistor to couple between said first gain control transistor and said differential amplifier.

6. The transimpedance amplifier of claim 1, wherein said input includes a first amplifier input, said amplifier further comprising a second input and a first feedback resistor connected across a first of said amplifier outputs and said first input, and a second feedback resistor connected across a second of said amplifier outputs and said second amplifier input.

7. The transimpedance amplifier of claim 1, wherein said first peak detector is configured to detect peak amplitudes associated with signals at said amplifier outputs.

8. The transimpedance amplifier of claim 1, wherein said second peak detector is configured to generate a reference signal associated with said differential amplifier outputs.

9. The transimpedance amplifier of claim 1, wherein said first peak detector comprises a first and second transistors, said first transistor to couple to a first of said amplifier outputs, said second transistor to couple to a second of said amplifier inputs.

10. The transimpedance amplifier of claim 9, wherein said first peak detector further comprises a third transistor to couple to said first and second transistors, said third transistor configured to receive a bias signal to control detection of a differential voltage swing between output signals of said differential amplifier.

11. The transimpedance amplifier of claim 1, wherein said second peak detector includes a first and second transistors, said first transistor to couple to a first output of said low pass filter, said second transistor to couple to a second output of said low pass filter.

12. The transimpedance amplifier of claim 11, further including a third transistor to couple to said first and second transistors, said third transistor configured to receive a bias signal to control the nominal threshold voltage of said first peak detector.

13. A transimpedance amplifier, comprising:

a differential amplifier having an input, a feedback input and outputs;

an automatic gain control circuit connected across the input and outputs of said differential amplifier for controlling the impedance of said differential amplifier; and

an offset control circuit, independent of said automatic gain control circuit, connected between said amplifier feedback input and said amplifier outputs, said offset control circuit configured to correct offset associated with said differential amplifier.

14. The transimpedance amplifier of claim 13, wherein said offset control circuit comprising:

a low pass filter to couple to said differential amplifier outputs;

an integrator to couple to said low pass filter; and

a transistor to couple to said integrator configured to have a current proportional to said offset associated with said differential amplifier.

15. The transimpedance amplifier of claim 13, wherein said automatic gain control circuit comprising:

a direct current gain amplifier;

a first peak detector to couple between said amplifier outputs and said direct current gain amplifier configured to detect peak amplitudes associated with differential amplifier output signals; and

a second peak detector to couple to said direct current gain amplifier.

16. The transimpedance amplifier of claim 15, wherein said automatic gain control circuit further comprises a plurality of gain control transistors to couple between said differential amplifier and said direct current gain amplifier.

17. The transimpedance amplifier of claim 1, wherein said transimpedance amplifier is connected to a transmission medium configured to allow propagation of optical signals.

18. A system, comprising:

a transmission medium configured to allow propagation of information signals;

an optical to electrical converter for receiving optical signals and generating a current signal proportional to said received optical signals; and

a transimpedance amplifier operatively responsive to said optical to electrical converter, said transimpedance amplifier having an automatic gain control circuit for controlling said transimpedance amplifier and an offset correction circuit for correcting the offset voltage associated with said transimpedance amplifier , said automatic gain control circuit being independent from said offset correction circuit.

19. The system of claim 18, wherein said automatic gain control circuit comprises first peak detector to couple to a first and second outputs of said transimpedance amplifier, said first peak detector configured to detect peak amplitude voltages associated with said transimpedance amplifier.

20. The system of claim 19, further comprising:

a low pass filter to couple to said TIA outputs; and

a second peak detector to couple to said low pass filter, said second peak detector configured to produce a reference voltage associated with said TIA.